M16C/6N Group

Differences between M16C/6NA and M16C/6N4

1. Abstract

This document describes the differences between M16C/6NA and M16C/6N4 groups.

2. Introduction

The explanation of this document is applied to the following condition:
Applicable MCU: M16C/6NA, M16C/6N4

3. Contents

3.1 Function differences

Table 3.1.1 and table 3.1.2 show the function differences (mask ROM version and flash memory version). Table 3.1.3 shows the function differences (flash memory version).

Table 3.1.1 Function differences (mask ROM version and flash memory version)-1(Note1)

Item		M16C/6NA	M16C/6N4
Shortest instruction execution time		62.5ns(f(X_{IN})=16MHz, V_{CC}=4.2 to 5.5V)	50ns(f(BCLK)=20MHz, V_{CC}=4.0 to 5.5V)
Clock generating circuit		X_{IN}, X_{CIN}, on-chip oscillator When placed in low power mode, the divided-n value for the main clock does not change.	PLL, X_{IN}, X_{CIN}, on-chip oscillator When placed in low power mode, a divided-8 value is used for these clocks. The X_{IN} drive capability is set to HIGH.
Low power consumption		60mA (V_{CC}=5V, f(X_{IN})=16MHz without software wait, mask version)	18mA (V_{CC}=5V, f(BCLK)=20MHz, 1/1 prescaler, without software wait, mask version)
Memory expansion mode and microprocessor mode	Internal reserved area (Note 2)	Depend on the mode	M16C/6NA's internal reserved area + 27000_{16} to $27FFF_{16}$
	Address bus and I/O port	P4_0 to P4_3: Switchable between address bus and I/O port	P4_0 to P4_3, P3_4 to P3_7: Switchable between address bus and I/O port
Access to SFR		1 wait fixed	Variable (1 to 2 waits)
Software wait to external area		Variable (0 to 2 wait)	Variable (0 to 3 waits)
Protect (PRCR register)	Protected by the PRC0bit	CM0, CM1, CM2, PCLKR, CCLKR	CM0, CM1, CM2, PLC0, PCLKR, CCLKR
	Protected by the PRC1bit	PM0, PM1	PM0, PM1, PM2, TB2SC, INVC0, INVC1
	Protected by the PRC2bit	PD7, PD9, S3C	PD7, PD9, S3C
Watchdog timer		Watchdog timer interrupt No count source protective mode	Watchdog timer interrupt or watchdog timer reset is selected Count source protective mode is available
Address match interrupt		2	4

Note1: For details and characteristics, refer to hardware manual. When switching to M16C/6N4 group, conduct the equivalent of system evaluation tests conducted in M16C/6NA group.
Note2: The PM1 register's PM13 bit differs in the value after reset.

Table 3.1.2 Function differences (mask ROM version and flash memory version)-2(Note1)

Item	M16C/6NA	M16C/6N4
Timer A two-phase pulse signal processing	No function Z-phase (counter reset) input	Function Z-phase (counter reset) input
Timer functions for three-phase motor control	No function protected by protect register Dead time timer count source is fixed at f_2 divided by 2	Function protect by protect register Dead time timer count source is selected: f_1, f_1 divided by 2 Output polarity change, carrier wave phase detection, three-phase output forcible shutoff function by $\overline{NMI}$ input are available
Serial I/O (Note 2) (UART0 to UART2)	(UART, Clock synchronous) x 2 (UART, Clock synchronous, I^2C bus, IEBus) x 1	(UART, Clock synchronous, I^2C bus, IEBus) x 3
Serial I/O $\overline{RTS}$ timing	Assert low when reception is completed	Assert low when receive buffer is read
UART2 data transmit timing	After data was written, transfer starts at the 1st BRG overflow timing (Output starts one cycle of BRG overflow earlier than UART0 and UART1)	After data was written, transfer starts at the 2nd BRG overflow timing (same as UART0 and UART1)
Serial I/O Sleep function	Have	None
Serial I/O I^2C mode	Start condition, stop condition: Not auto-generation	Start condition, stop condition: Auto-generation
Serial I/O I^2C mode SDA delay	Only analog delay is selected as SDA delay. SDA digital delay count source: $1/f(X_{IN})$	Only digital delay is selected as SDA delay SDA digital delay count source: BRG
SI/O3 Clock polarity	Fixed	Selectable
A-D converter operation clock	Selectable: f_{2AD}, $f_{2AD}/2$, $f_{2AD}/4$	Selectable: f_{AD}, f_{AD} divided by 2, 3, 4, 6, 12
CAN CPU interface sleep function	None	CAN0 and CAN1 can select CPU interface operating or sleeping respectivly
CAN error interrupt CAN wake up interrupt	- CAN0/1 error interrupt - CAN0/1 wake up interrupt	Switchable - CAN0/1 error interrupt ,CAN0/1 wake up interrupt and - CAN0 error interrupt, CAN0 wake up interrupt and CAN1 error interrupt, CAN1 error interrupt
Condition of CAN wake up interrupt	CAN wake up interrupt occurs regardless of CAN operation mode	When CAN module enters CAN sleep mode, CAN wake up interrupt occurs.

Note1: For details and characteristics, refer to hardware manual. When switching to M16C/6N4 group, conduct the equivalent of system evaluation tests conducted in M16C/6NA group.
Note2: I^2C-bus is a trademark of Philips. IEBus is a trademark of NEC Electronics.

Table 3.1.3 Function differences (flash memory version)(Note1)

Item	M16C/6NA	M16C/6N4
User ROM blocks	7 blocks: 8Kbytes X 2, 16 Kbytes X 1, 32 Kbytes X 1, 64 Kbytes X 3 (Flash memory: max. 256 Kbytes)	9 blocks: 4 Kbytes X 2, 8 Kbytes X 3, 32 Kbytes X 1, 64 Kbytes X 3 (Flash memory: max. 256 Kbytes)
Data ROM area	None	Have
Program manner	Page	Word
Program command (Software command)	Page program command: have Program command: none (Program method: in units of page)	Page program command: none Program command: have (Program method: in units of word, in units of byte)
Block status after program function	Have	None
CPU rewrite mode	No EW1 mode	EW1 mode is available

Note1: For details and characteristics, refer to hardware manual. When switching to M16C/6N4 group, conduct the equivalent of system evaluation tests conducted in M16C/6NA group.

4. Website and Contact Information for Technical Support

Renesas Technology Corporation Semiconductor Home Page
http://www.renesas.com

CAN MCU Technical support
Customer support center: csc@renesas.com

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